CUSTOMER NO.: 24498
Serial No.: 10/551,084
Final Office Action Dated: March 13, 2008

PATENT
PU030099

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant: Robert Allen Castlebary

Examiner: Portka, Gary J.

Serial No: 10/551,084

Group Art Unit: 2188

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For: ASYNCHRONOUS JITTER REDUCTION TECHNIQUE

Mail Stop Appeal Brief-Patents
Hon. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Applicant appeals the status of claims 1-12 as presented in response to the Final Office Action dated March 13, 2008 pursuant to the Notice of Appeal filed June 11, 2008 and submit this appeal brief.

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via facsimile to Mail Stop Amendment, Commissioner for Patents, at facsimile number (571) 273-8300 on Aug. 6, 2008

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D1. Claims 2-5 are patentable over Stern and Spalink, as the references do not disclose or render obvious the feature of applying read clock pulses to the memory recited in the claims at a frequency that is a whole number multiple of a write clock frequency or the feature of altering the duration of a Read Address.

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1. **Real Party in Interest**

The real party in interest is GRASS VALLEY (U.S.) INC., the assignee of the entire right title and interest in and to the subject application by virtue of an assignment recorded with the Patent Office on September 27, 2005 at reel/frame 017832/0966.

2. **Related Appeals and Interferences**

None.

3. **Status of Claims**

Claims 1-12 are pending. Claims 1-12 stand rejected and are under appeal.

A copy of the claims 1-12 is presented in Section 8 below.

4. **Status of Amendments**

An amendment under 37 CFR §1.111, sent to the PTO on December 6, 2007 in response to the non-final Office Action dated October 3, 2007, was entered. An amendment under 37 C.F.R. §1.116, sent to the PTO on May 9, 2008 in response to the final Office Action dated March 13, 2008, was also entered. No Responses/Amendments were filed subsequent to the Amendment sent to the PTO on May 9, 2008.

5. **Summary of Claimed Subject Matter**

Claim 1 is directed to a method for reading data from a memory to achieve reduced jitter, including the steps of: applying successive read clock pulses to the memory at a

frequency of $x f_n$ where x is a whole integer and f_n is the frequency at which the memory is clocked to write data (see, e.g.,. Specification, FIG. 5; p. 4, lines 24-26; p. 2, lines 31-33; p. 2, lines 24-27); applying successive Read Addresses to the memory at a rate slower than the xf_n frequency of said applying successive read clock pulses to identify successive locations in the memory for reading when the memory is clocked with read clocked pulses to enable reading of samples stored at such successive locations (see, e.g., Specification, p. 4, lines 27-29; p. 2, lines 29-34; FIG. 1, elements 12, 22, 24, 26, 30); and altering the duration of at least one successive Read Addresses in response to memory usage status to maintain memory capacity below a prescribed threshold (see, e.g.,. Specification, FIG. 5; p. 4, line 31 to p. 5, line 11; p. 2, lines 31-33; p. 2, lines 24-27).

Claim 7 is directed to system for reading stored data to achieve reduced jitter including: a memory (see, e.g., Specification, FIG. 1, element 12) into which data is written and from which data is read (see, e.g., Specification, FIG. 2, FIG. 5; p. 2, lines 24-27; p. 2, lines 31-33); a clock (see, e.g., Specification, FIG. 1, element 25) applying successive read clock pulses to the memory at a frequency of $x f_n$ where x is a whole integer and f_n is the frequency at which the memory is clocked to write data (see, e.g., Specification, FIG. 5; p. 4, lines 24-26; p. 2, lines 31-34; p. 2, lines 24-27); and a memory address generator (see, e.g., Specification, FIG. 1, element 30) for applying successive Read Addresses to the memory at a rate slower than the xf_n frequency of said clock applying successive read clock pulses to identify successive locations in the memory for reading when the memory is clocked with read clocked pulses to enable reading of samples stored at such successive locations (see, e.g., Specification, p. 4, lines 27-29; p. 2, lines 29-45; FIG. 1, elements 12, 22, 24, 26, 30); and for

altering the duration of at least one successive Read Addresses in response to memory usage status to maintain memory capacity below a prescribed threshold (see, e.g., Specification, FIG. 5; p. 4, line 31 to p. 5, line 11; p. 2, lines 31-33; p. 2, lines 24-27).

6. Grounds of Rejection to be Reviewed on Appeal

Claims 1, 6, 7 and 12 stand rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 4,805,198 to Stern et al. (hereinafter 'Stern').

Claims 2-5 and 8-11 stand rejected under 35 U.S.C. §103(a) over Stern in view of U.S. Publication No. 2007/0116062 (hereinafter 'Spalink').

The preceding rejections are presented for review in this Appeal.

Regarding the grouping of the claims, claims 2-6 stand or fall with claim 1 due to their respective dependencies. In addition, claims 8-12 stand or fall with claim 7 due to their respective dependencies.

7. Argument

A. Introduction

In general, implementations of the present principles are directed to reducing jitter resulting from writing to and reading from a memory device. According to one aspect of the present principles, write clock pulses and read clock pulses are applied to the memory to signal when the memory should be written to and read from, respectively (see, e.g., Specification, p.1, lines 15-18). In addition, successive read addresses can be applied to the memory to identify locations from which data is read according to read clock pulses (see, e.g., Specification, p. 2,

lines 29-34). Further, read clock pulses can be applied to the memory at a frequency that is a whole number multiple (x) of a write clock frequency (f_n) to reduce jitter (see, e.g., Specification, p. 4, lines 23-27).

For example, with reference to FIGS. 2-4 and FIG. 5, illustrating prior art systems and one implementation of the present principles, respectively, because higher frequency pulses are applied, part of a memory address (e.g., n+1 or n+2) may be repeated or skipped to correct for jitter as opposed to repeating or skipping an entire memory address, as applied in the prior art (see, e.g., Specification, p. 4, line 31 to p. 5, line 9). As a result of altering the duration or length of the memory address in this way, any jitter observed is lessened because disparity or error in the data sequence read is reduced (see, e.g., Specification, p. 4, line 31 to p. 5, line 9).

Independent claims 1 and 7 of the present application include the features of applying read clock pulses to the memory at a frequency that is a whole number multiple of a write clock frequency and altering the duration of a Read Address. The art of record does not disclose or render obvious either of these features. Accordingly, the claims of the present application are not anticipated or render obvious by the cited references. As such, claims 1 and 7 are presented for review in this appeal.

B. Whether claims 1 and 6 are unpatentable under 35 U.S.C. §102(b) in view of Stern.

Claims 1 and 6 are patentable under 35 U.S.C. §102(b) in view of Stern, as Stern fails to teach each and every element included therein. First, Stern does not disclose the feature of applying read clock pulses to the memory recited in the claims at a frequency that is a whole

number multiple of a write clock frequency. Second, Stern does not teach the feature of altering the duration of a Read Address. Thus, claims 1 and 6 are patentable over Stern.

B1. Claims 1 and 6 are patentable over Stern, as Stern does not teach the element of applying read clock pulses to the memory recited in the claims at a frequency that is a whole number multiple of a write clock frequency.

Because Stern does not disclose or render obvious the feature of applying read clock pulses to the memory recited in the claims at a frequency that is a whole number multiple of a write clock frequency, claims 1 and 6 are not anticipated by Stern. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Independent claim 1 recites:

> A method for reading data from a memory to achieve reduced jitter, comprising the steps of:
>
> applying successive read clock pulses to the memory at a frequency of x f_n where x is a whole integer and f_n is the frequency at which the memory is clocked to write data;
>
> applying successive Read Addresses to the memory at a rate slower than the xf_n frequency of said applying successive read clock pulses to identify successive locations in the memory for reading when the memory is clocked with read clocked pulses to enable reading of samples stored at such successive locations; and
>
> altering the duration of at least one successive Read Addresses in response to memory usage status to maintain memory capacity below a prescribed threshold.

(emphasis added).

Stern does not disclose or render obvious at least the element of applying read clock pulses to the memory recited in the claims at a frequency that is a whole number multiple of a write clock frequency. As recited in claim 1, Read Addresses are applied to a memory to

identify memory locations from which samples are read in accordance with read clock pulses. The Stern patent describes a memory comprised of storage cells 60-75 of FIG. 2A whose addresses are read in accordance with a read clock pulse (element 32) provided by means of an address pointer (see, e.g., Stern column 9, lines 21-32; column 10, lines 7-16; column 3, lines 55-60). While the frequency of the read clock signal can be altered (see, e.g. Stern, column 3, line 61 to column 4, line 12), the read clock signal frequency is not a whole number multiple of a write clock frequency. Rather, the read clock signal is on the same order as the write clock frequency (see, e.g., Stern FIG. 1; column 3 lines 26-31; column 3, lines 45-49) (describing the frequency of read clock signal 32 as being one-forth the frequency of a 4X clock 28, which is four times the write clock frequency). Thus, Stern does not disclose or render obvious applying read clock pulses to the memory recited in the claims at a frequency that is a whole number multiple of a write clock frequency.

Furthermore, although Stern describes employing a 4X signal 28 having a frequency that is a multiple of a write clock signal, the 4X signal 28 is not applied to a memory as recited in claim 1. As stated above, the memory recited in claim 1 has successive read addresses applied to it to identify locations from which data is read according to read clock pulses. The 4X signal 28 is not applied to any such memory. The 4X signal 28 is employed within a capacitor control logic to facilitate altering the frequency of an oscillator (see, e.g., Stern, column 11, line 55 to column 12, line 4). Nowhere does Stern disclose or render obvious that read clock pulses with a frequency that is a whole number multiple of a write clock frequency is applied to a memory as recited in claim 1.

Accordingly, claim 1 is not anticipated by Stern, as Stern does not disclose each and every element recited therein. Moreover, claim is not anticipated by Stern due at least to its dependency on claim 1. As such, claims 1 and 6 are patentable over Stern.

B2. Claims 1 and 6 are patentable over Stern because Stern does not teach the element of altering the duration of at least one successive Read Address.

As Stern does not disclose or render obvious the feature of altering the duration of at least one successive Read Address, claims 1 and 6 are not anticipated by Stern. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," as stated above. Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Independent claim 1 recites:

> A method for reading data from a memory to achieve reduced jitter, comprising the steps of:
>
> applying successive read clock pulses to the memory at a frequency of x f_n where x is a whole integer and f_n is the frequency at which the memory is clocked to write data;
>
> applying successive Read Addresses to the memory at a rate slower than the xf_n frequency of said applying successive read clock pulses to identify successive locations in the memory for reading when the memory is clocked with read clocked pulses to enable reading of samples stored at such successive locations; and
>
> altering the duration of at least one successive Read Addresses in response to memory usage status to maintain memory capacity below a prescribed threshold.
>
> (emphasis added).

Stern does not disclose or render obvious at least the claim element of altering the duration of at least one Read Address. As discussed in the Specification of the present

application with regard to FIG. 5, altering the "duration" of a "Read Address" corresponds to varying the fraction or quantity of data read from a storage address at a particular read instance:

> To compensate for a lack of synchronism between reading and writing of data, the multi-bit counter 30 varies the length of one or more addresses to skip or repeat a fraction of a sample in accordance with the usage status of the FIFO 12 to prevent over flow or under flow, and thus maintain the FIFO capacity with prescribed threshold limits. As shown on line (c), the duration (length) of at least one read address (e.g. read address (n+2) is skipped to skip a fraction of a sample (e.g., a 1/4 sample), as shown in line (b) of FIG. 5, to compensate when the reading of data from the FIFO 12 lags the writing of data. Referring to line (e) of FIG. 5, the duration of at least one read address (e.g. read address (n+2) is lengthened to repeat a fraction of a sample (e.g., a 1/4 sample), as shown in line (d) of FIG. 5, to compensate when the writing of data from the FIFO 12 lags the reading of data. By increasing the Read Clock frequency in the manner described above, the jitter caused by repeating or skipping a sample becomes 1/x of the clock cycle, rather than a whole clock pulse as in the case with the prior art approach illustrated in FIGS. 3 and 4.

(Specification, p. 4, line 31 to p. 5, line 9) (emphasis added). (see also, Specification, FIG. 5). Stern nowhere discloses or renders obvious altering the duration of a Read Address because varying the fraction of data read from a storage address in the Stern system is not possible. The Stern patent describes a 16-bit FIFO (First in First Out) register having 16 storage cells or storage addresses, each of which stores a single bit (see, e.g., Stern, column 4, lines 52-56; column 2, lines 60-62; and column 3, lines 64 to column 4, line 12). A single bit is the smallest denomination of data and, as such, cannot be partitioned. Thus, because each storage address in Stern has a one-bit capacity, the fraction or quantity of data read from a storage address cannot be varied. If data is read from a storage address of the Stern system, only the whole bit can be read. Accordingly, Stern does not disclose that the length or duration of at least one read address is altered.

In contrast, according to aspects of the present principles, at the time of filing of the Application, as well-known in the art, a storage address corresponds to the storage location of a byte of data including multiple bits. In implementations of the present principles a multi-bit counter alters the duration of a Read Address by varying the fraction or quantity of data read from a storage address at a particular read instance, as discussed at length above (see, e.g., Specification, p. 4, lines 31-34).

Accordingly, claim 1 is not anticipated by Stern at least because Stern does not disclose the feature of that the length or duration of at least one storage address is altered. In addition, claim 6 is not anticipated by Stern due at least to its dependency on claim 1. As such, claims 1 and 6 are patentable over Stern. Withdrawal of the rejection is respectfully requested.

C. Whether claims 7 and 12 are unpatentable under 35 U.S.C. §102(b) in view of Stern.

C1. Claims 7 and 12 are patentable over Stern, as Stern does not disclose the feature of applying read clock pulses to the memory recited in the claims at a frequency that is a whole number multiple of a write clock frequency or the feature of altering the duration of a Read Address.

Because Stern fails to anticipate the feature of applying read clock pulses to the memory recited in the claims at a frequency that is a whole number multiple of a write clock frequency or the feature of altering the duration of a Read Address, claims 7 and 12 are patentable over Stern. "A claim is anticipated only if each and every element as set forth in the claim is found, either

expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Claim 7 recites:

> A system for reading stored data to achieve reduced jitter, comprising:
> a memory into which data is written and from which data is read;
> a clock applying successive read clock pulses to the memory at a frequency of $x f_n$ where x is a whole integer and f_n is the frequency at which the memory is clocked to write data;
> a memory address generator for applying successive Read Addresses to the memory at a rate slower than the xf_n frequency of said clock applying successive read clock pulses to identify successive locations in the memory for reading when the memory is clocked with read clocked pulses to enable reading of samples stored at such successive locations; and for altering the duration of at least one successive Read Addresses in response to memory usage status to maintain memory capacity below a prescribed threshold.

As discussed above, with regard to claim 1, Stern fails to disclose the element of applying read clock pulses to the memory recited in the claims at a frequency that is a whole number multiple of a write clock frequency or the element of altering the duration of a Read Address. Accordingly, claim 7 is not anticipated by Stern. In addition, claim 11 is not anticipated by Stern due at least to its dependency on claim 7. As such, claims 7 and 11 are patentable over Stern. Thus, withdrawal of the rejection is respectfully requested.

D. Whether claims 2-5 are Unpatentable under 35 U.S.C. §103(a) over Stern in view of Spalink.

D1. Claims 2-5 are patentable over Stern and Spalink, as the references do not disclose or render obvious the feature of applying read clock pulses to the memory recited in the claims at a frequency that is a whole number multiple of a write clock frequency or the feature of altering the duration of a Read Address.

Claims 2-5 are patentable over Stern and/or Spalink, as the references do not render obvious several features of the claims. Claimed subject matter is unpatentable under 35 U.S.C. 103(a) "if the differences between the subject matter sought to be protected and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." KSR International Co. v. Teleflex, Inc., 127 S.Ct.1727, 1734 (quoting 35 U.S.C. 103(a)). Claims 2-5 are dependent on claim 1. Thus, the subject matter of claims 2-5 includes:

> A method for reading data from a memory to achieve reduced jitter, comprising the steps of:
>
> applying successive read clock pulses to the memory at a frequency of x f_n where x is a whole integer and f_n is the frequency at which the memory is clocked to write data;
>
> applying successive Read Addresses to the memory at a rate slower than the xf_n frequency of said applying successive read clock pulses to identify successive locations in the memory for reading when the memory is clocked with read clocked pulses to enable reading of samples stored at such successive locations; and
>
> altering the duration of at least one successive Read Addresses in response to memory usage status to maintain memory capacity below a prescribed threshold.

(emphasis added).

As discussed above, Stern fails to disclose the features of: (a) applying read clock pulses to the memory recited in the claims at a frequency that is a whole number multiple of a write clock frequency, and (b) altering the duration of a Read Address. The Spalink patent likewise fails to disclose these features. Spalink is directed to synchronizing cycle times employed by various IEEE 1394 nodes in a network (see, e.g., Spalink Abstract; paragraph. 18). Spalink does not describe or suggest applying any read clock pulses to a memory at a frequency that is a whole number multiple of a write clock frequency. In addition, although Spalink describes

inserting or skipping clocks to correct a timing cycle at a network node (see, e.g., Spalink, paragraph. 30) Spalink nowhere discloses or remotely suggests that inserting or skipping a clock in any way correlates to varying the fraction or quantity of data read from a storage address at a particular read instance, as discussed above. Thus, Spalink also does not disclose or render obvious altering the "duration" of a "Read Address," as recited in the claims. Moreover, combination of Spalink with Stern would not render obvious altering the "duration" of a "Read Address" because such a feature is not even in the Stern system, as discussed above.

Accordingly, claims 2-5 are patentable over Stern and/or Spalink for at least the reasons stated above. Withdrawal of the rejection is respectfully requested.

E. Whether claims 8-11 are Unpatentable under 35 U.S.C. §103(a) over Stern in view of Spalink.

E1. Claims 8-11 are patentable over Stern and Spalink, as the references do not disclose or render obvious the feature of applying read clock pulses to the memory recited in the claims at a frequency that is a whole number multiple of a write clock frequency or the feature of altering the duration of a Read Address.

Because Stern and Spalink fail to render obvious the feature of applying read clock pulses to the memory recited in the claims at a frequency that is a whole number multiple of a write clock frequency or the feature of altering the duration of a Read Address, claims 8-11 are patentable over Stern and Spalink, taken singly or in combination. Claimed subject matter is unpatentable under 35 U.S.C. 103(a) "if the differences between the subject matter sought to be protected and the prior art are such that the subject matter as a whole would have been obvious

at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." KSR International Co. v. Teleflex, Inc., 127 S.Ct.1727, 1734 (quoting 35 U.S.C. 103(a)). Claims 8-11 are dependent on claim 7. Thus, the subject matter of claims 8-11 includes:

> A system for reading stored data to achieve reduced jitter, comprising:
> a memory into which data is written and from which data is read;
> a clock applying successive read clock pulses to the memory at a frequency of $x f_n$ where x is a whole integer and f_n is the frequency at which the memory is clocked to write data;
> a memory address generator for applying successive Read Addresses to the memory at a rate slower than the xf_n frequency of said clock applying successive read clock pulses to identify successive locations in the memory for reading when the memory is clocked with read clocked pulses to enable reading of samples stored at such successive locations; and for altering the duration of at least one successive Read Addresses in response to memory usage status to maintain memory capacity below a prescribed threshold.

(emphasis added).

As discussed above with regard to claims 2-5, neither of Stern or Spalink discloses or renders obvious the element of applying read clock pulses to the memory recited in the claims at a frequency that is a whole number multiple of a write clock frequency or the element of altering the duration of a Read Address. Accordingly, claim s 8-11 are patentable over Stern and/or Spalink, as the references do not render the claims obvious. As such, withdrawal of the rejection is respectfully requested.

F. Conclusion

At least the above-identified limitations of the pending claims are not disclosed or rendered obvious by the teachings of Stern and/or Spalink. Accordingly, it is respectfully requested that the Board reverse the rejection of claims 1-12.

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Respectfully submitted,
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8. CLAIMS APPENDIX

1. (Previously presented) A method for reading data from a memory to achieve reduced jitter, comprising the steps of:

applying successive read clock pulses to the memory at a frequency of $x f_n$ where x is a whole integer and f_n is the frequency at which the memory is clocked to write data;

applying successive Read Addresses to the memory at a rate slower than the xf_n frequency of said applying successive read clock pulses to identify successive locations in the memory for reading when the memory is clocked with read clocked pulses to enable reading of samples stored at such successive locations; and

altering the duration of at least one successive Read Addresses in response to memory usage status to maintain memory capacity below a prescribed threshold.

2. (Original) The method according to claim 1 further comprising the step of lengthening the duration of the at least one Read Address to repeat reading of a fractional sample.

3. (Original) The method according to claim 2 further comprising the step of lengthening the duration of more than one Read Address to repeat the reading of more than one fractional sample.

4. (Original) The method according to claim 1 further comprising the step of

shortening the duration of the at least one Read Address to skip reading of a fractional sample.

5. (Original) The method according to claim 4 further comprising the step of shortening the duration of more than one Read Address to skip reading of more than one fractional sample.

6. (Original) The method according to claim 1 further comprising the step of applying the successive read clock pulses to the memory at a frequency four times the frequency f_n.

7. (Previously presented) A system for reading stored data to achieve reduced jitter, comprising:

a memory into which data is written and from which data is read;

a clock applying successive read clock pulses to the memory at a frequency of $x f_n$ where x is a whole integer and f_n is the frequency at which the memory is clocked to write data;

a memory address generator for applying successive Read Addresses to the memory at a rate slower than the xf_n frequency of said clock applying successive read clock pulses to identify successive locations in the memory for reading when the memory is clocked with read clocked pulses to enable reading of samples stored at such successive locations; and for altering the duration of at least one successive Read Addresses in response to memory usage status to maintain memory capacity below a prescribed threshold.

8. (Original) The apparatus according to claim 7 wherein the memory address generator lengthens the duration of the at least one Read Address to repeat reading of a fractional sample.

9. (Original) The apparatus according to claim 8 wherein the memory address generator lengthens the duration of more than one Read Address to repeat the reading of more than one fractional sample.

10. (Original) The apparatus according to claim 7 wherein the memory address generator shortens the duration of the at least one Read Address to skip reading of a fractional sample.

11. (Original) The apparatus according to claim 10 wherein the memory address generator shortens the duration of more than one Read Address to skip reading of more than one fractional sample.

12. (Original) The apparatus according to claim 1 wherein the system clock applies successive read clock pulses to the memory at a frequency four times the frequency f_n.

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9. RELATED EVIDENCE APPENDIX

None.

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10. RELATED PROCEEDINGS APPENDIX

None